WHAT IS CLAIMED IS:

1. A semiconductor fabrication process, comprising:

forming a gate electrode over a gate dielectric over a semiconductor substrate;

depositing a spacer film over the gate electrode, the deposited spacer film exhibiting a first tensile stress;

modulating a stress characteristic of at least a portion of the spacer film from the first tensile stress to a second tensile stress; and

etching the spacer film to form sidewall spacers laterally disposed on either side of the gate electrode, wherein at least a portion of the sidewall spacers include sidewall spacers exhibiting the second tensile stress.

2. The process of claim 1, wherein depositing the spacer film comprises thermally depositing silicon nitride at a temperature in the range of approximately 550 to 750 °C.

3. The process of claim 1, wherein modulating the stress characteristic comprises implanting a species into at least a portion of the spacer film.

4. The process of claim 3, wherein the ion implanting includes implanting Xenon into at least a portion of the spacer film.

5. The process of claim 4, wherein implanting Xenon further includes implanting Xenon into portions of the spacer film over p-channel transistors.

6. The process of claim 5, wherein implanting Xenon still further includes implanting Xenon at an energy of at least 180 keV.

7. The process of claim 5, wherein implanting Xenon still further includes implanting at an implant angle of approximately 45°.

8. The process of claim 3, wherein the ion implanting includes implanting Germanium into the spacer film.

9. The process of claim 8, wherein implanting Germanium further includes implanting Germanium at an energy of at least 80 keV and an implant angle of approximately 10°.

10. A semiconductor fabrication process, comprising:

depositing a silicon nitride spacer film over a gate electrode and a semiconductor substrate over which the gate electrode is positioned;

etching the spacer film to form silicon nitride spacers on sidewalls of the gate electrode; and

implanting at least some of the sidewall spacers with an implant species to modulate a stress characteristic of the implanted spacers.

11. The process of claim 10, wherein depositing silicon nitride further includes depositing silicon nitride exhibiting a first tensile stress characteristic.

12. The process of claim 11, wherein depositing silicon nitride still further includes depositing silicon nitride with a thermal CVD process in which the deposition temperature is in the range of approximately 550 to 750 °C.

13. The process of claim 11, wherein implanting at least some of the sidewall spacers still further includes implanting a species selected from Xenon and Germanium into the at least some of the sidewall spacers using an implant angle of 10° or greater.

14. The process of claim 13, wherein implanting at least some of the sidewall spacers still further includes implanting with an implant energy not less than 80 keV.

15. The process of claim 11, wherein implanting at least some of the sidewall spacers still further includes selectively implanting portions of at least some of the sidewall spacers of n-channel transistors with Xenon ions at an implant energy of approximately 180 keV and an implant angle of approximately 45°.

16. The process of claim 10, wherein implanting the at least some of the sidewall spacers still further includes blanket implanting the at least some of the sidewall spacers with Germanium at an implant energy of 80 keV and an implant angle of approximately 10°.

17. An integrated circuit, comprising:

first and second transistors, each including a gate electrode over a gate dielectric over a semiconductor substrate;

first spacer structures adjacent sidewalls of the first gate electrode and second spacer structures adjacent sidewalls of the second gate electrode; and

first source/drain regions within the substrate and self-aligned to the first spacer structures and second source/drain regions within the substrate and self-aligned to the second spacer structures, wherein the first and second sidewall spacer structures comprise silicon nitride having a Si/N ratio of less than 0.8 and further wherein the first sidewall spacer structures include a distribution of an impurity selected from Xenon and Germanium.

18. The integrated circuit of claim 17, wherein the second sidewall spacer structures exhibit a tensile stress characteristic that is greater than a corresponding characteristic of the first spacer structure.

19. The integrated circuit of claim 18, wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor.

20. The integrated circuit of claim 17, wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor and wherein the second sidewall spacer structures further include a distribution of an impurity selected from Xenon and Germanium.